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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,925	07/07/2003	Takahiro Kawano	239801US2	6929

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,925	KAWANO ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41,43 and 44* is/are pending in the application.

4a) Of the above claim(s) *2,3,7-20 and 25-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,21-24,39-41,43 and 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6, 21-24, 39-41 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. (6,316,814) in view of Applicant Admitted Prior Art (AAPA).

Nagata et al. teach in figure 1A and related text a semiconductor device comprising:

a semiconductor layer which includes a first semiconductor region 14 of a first conductivity type, a base region 12 of a second conductivity type, and a plurality of second semiconductor regions 20 of the first conductivity type;

a gate wiring 13 which is formed on the semiconductor layer via a first insulating film;

a plurality of main electrodes 15A (or the electrode located just below line 15A, see also figure 1B) which are electrically connected to the plurality of second semiconductor regions and which are insulated from the gate wiring, wherein the gate wiring is arranged between the main electrodes and

upper surfaces of the main electrodes are higher than the highest portion of an upper surface of the gate wiring.

Nagata et al. do not teach a connecting plate which is directly connected onto the upper surfaces of the main electrodes.

AAPA teaches in figure 21 and related text (page 3, lines 9-10) a connecting plate 2109 is directly connected onto the upper surfaces of the main electrodes of the device 2105. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect a connecting plate directly onto the upper surfaces of the electrodes of Nagata et al.'s device in order to provide better electrical connection between the electrodes and the external wirings, and in order to reduce the contact resistance of the device.

Regarding the claimed limitations of main electrodes being in contact with a contact region of the connecting plates and in an area under the contact region of the connecting plates the upper surfaces of the main electrodes are higher than the highest portion of an upper surface of the gate wiring, these features are inherent in prior art's device because the main electrodes are connected to the connecting plates and they thus must be in contact with a contact region of the connecting plates. The area under the contact region of the connecting plates must be where the upper surfaces of the main electrodes are higher than the highest portion of an upper surface of the gate wiring, because the contact region must be located above the upper surfaces of the main electrodes.

Regarding claims 4, 21-23 and 39-41, AAPA teaches gate wiring 2107 comprising aluminum, and a connecting plate connected to a lead frame. It would have been

obvious to a person of ordinary skill in the art at the time the invention was made to form the main electrodes and the connecting plate of a plurality of metal layers comprising aluminum and to connect the connecting plate to a lead frame in Nagata et al.'s device in order to reduce the contact resistance between the main electrodes and the lead frame and in order to provide external connections to the device.

Regarding claim 4, Nagata et al. teach a second insulating film extends between plurality of metal layers.

Regarding claim 5, Nagata et al. teach in figure 1 plurality of main electrodes are formed apart from the gate wiring with a gap there between.

Regarding the process limitations recited in claims 23 and 41 ("the first connecting plate is connected to the first main electrode and the second main electrode by ultrasonic bonding") these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.
Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by

process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 6, 24 and 43, Nagata et al. teach a first gate electrode which is formed in the cell forming region and controls continuity between the first semiconductor region and the second semiconductor region; and first and second main electrodes (see the array in figure 1B) which are electrically connected to the plurality of second semiconductor regions respectively and which are formed at predetermined intervals in the cell forming region on the semiconductor layer.

Regarding claim 24, Nagata et al. do not teach a first semiconductor layer of a first conductivity type. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a first semiconductor layer of a first conductivity type in Nagata et al.'s device in order to improve the electrical isolation of the device.

Response to Arguments

Applicant argues that Vdd wiring layer 15A of Nagata et al. is not the main electrode, because Vdd wiring layer 15A is provided midway between a photoelectric conversion region 14 and a light shielding film 22A and formed in an interlayer insulating

film, and is disposed protruding into the inside of an aperture 23A when viewed from the top of the aperture to define the light admitting region.

The fact that Vdd wiring layer 15A of Nagata et al. is provided midway between a photoelectric conversion region 14 and a light shielding film 22A and formed in an interlayer insulating film, and is disposed protruding into the inside of an aperture 23A when viewed from the top of the aperture to define the light admitting region, does not preclude it from being called "main electrode".

Applicant argues that Nagata et al. do not teach or suggest the relationship between upper surfaces of the first and second main electrodes and the highest portion of the gate wiring, because the light shielding film 22A is not directly connected to upper surfaces of electrode 15A.

Light shielding film 22A was not cited in the rejection of the claimed invention.

Applicant argues that Nagata et al. do not teach or suggest that wiring layer 13 is arranged between the wiring layers 15A, because figure 1 clearly show that wiring layer 13 is underneath wiring layer 15A.

Although figure 1 depicts wiring layer 13 is underneath wiring layer 15A, it does not preclude wiring layer 13 from being arranged between the wiring layers 15A. Figure 1B depicts an array of wiring layers, wherein wiring layers 13 and 15A are alternatively formed such that wiring layer 13 is arranged between the wiring layers 15A, as claimed.

Applicant argues that figure 21 of AAPA does not show any electrodes directly connected to a connecting plate as required by claims 1, 6, and 24, because figure 21 shows a void between connecting plate 2109 and a source electrode 2105.

Although figure 21 depicts a void between connecting plate 2109 and a source electrode 2105, the disclosure (page 3, lines 9-10) explicitly states that electrode 2105 is directly connected to a connecting plate as required by claims 1, 6, and 24.

Conclusion

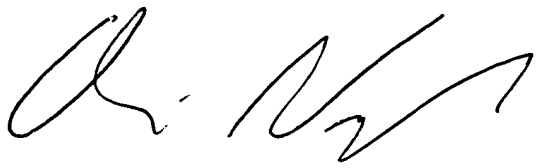
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



O.N.
2/1/06

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